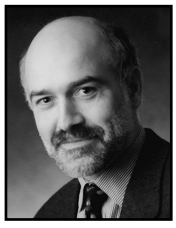
Tutorials

T1: Embedded Power-Management Circuits

Due to the drastic increase of system integration and power consumption of an IC with technology scaling, power management becomes a critical issue in determining the overall performance of the IC. This tutorial starts with a brief overview of power management circuits for embedded applications. There follows a detailed explanation of the operation and design issues associated with various on-chip power converter circuits including linear regulator, switched-inductor regulator, and switched-capacitor regulator. The focus is on the analog circuit techniques, and the control mechanism for implementing these power converters.

Instructor: Philip K.T. Mok received his B.A.Sc., M.A.Sc., and Ph.D. degrees in electrical and computer engineering from the University of Toronto, Toronto, ON, Canada, in 1986, 1989, and 1995, respectively. In January 1995, he joined the Department of Electronic and Computer Engineering at the Hong Kong University of Science and Technology, Hong Kong, China, where he is currently an Associate Professor. His current research interests include power-management integrated circuits and low-voltage analog integrated-circuits. He received the Henry G. Acres Medal, the W.S. Wilson Medal, and a Teaching-Assistant Award from the University of Toronto, and the Teaching Excellence Appreciation Award twice from The Hong Kong University of Science and Technology. He has served on the ISSCC analog sub-committee since 2005 and is an associate editor for the IEEE Transactions on Circuits and Systems II and the Journal of Solid-State Circuits since 2006.



T2: Continuous-Time $\Delta\Sigma$ Data Converters

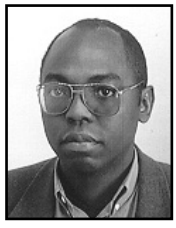
While technologies are continuing to provide us with ever faster transistors they also demand that we work at lower supply voltages. The analog designer has to search for new concepts to counteract the reduction of signal swings and increase in power. Although time-continuous circuits are anything but new, they are gaining a renewed interest not only in the academic, but also in the industrial community. With the main focus on baseband applications, different aspects of continuous-time $\Delta\Sigma$ modulators will be covered when operated under low-power and low-voltage constraints; Architectures for baseband applications; Implicit anti-aliasing filter; Influence of non-idealities and correction techniques; Implementations (low power, ultra wideband, high performance)

Instructor: Yiannos Manoli holds the Chair of Microelectronics at the University of Freiburg, Germany. His current research interests lie in the design of low-voltage and low-power mixed-signal CMOS circuits, sensor read-out circuits as well as A/D- and D/A-converters with over 150 papers in these areas. He holds a B.A. degree in Physics and Mathematics, a M.S. degree in electrical engineering and computer science from the University of California, Berkeley, and the Dr. Ing. Degree in electrical engineering from the Gerhard Mercator University in Duisburg, Germany.

T3: Dealing with Issues in VLSI Interconnect Scaling

Designers have recognized for many years that on-chip wires can limit system performance, and as technologies continue to scale, the problems posed by on-chip wires continue to worsen. This tutorial introduces models for the resistance, capacitance, and inductance of on-chip wiring and discusses metrics for the delay, bandwidth, noise performance, and energy costs of wires. We consider scaling trends several generations into the future, and how wires perform relative to transistors. We will also examine broader implications of wires for design and CAD tools, notably how they impact architectural trends for both custom and ASIC design flows. Finally, a number of promising design techniques and technologies that can improve the performance of on-chip communication are discussed.

Instructor: Ron Ho is a Senior Research Scientist at Sun Microsystems Laboratories in Menlo Park, CA, where he worries about the future of wires. He received his Ph.D. in electrical engineering from Stanford University. From 1993 to 2003, he was at Intel in Santa Clara, CA, where he worked on processors ranging from the 80486 to the 3rd-generation Itanium. In 2003, he joined Sun Labs, where he is currently researching high-performance and low-energy communication technologies, both on a single chip and between two chips. In 2005, he was also a Lecturer at Stanford University, where he taught a graduate class on circuit design.



T4: Dynamic Offset-Cancellation Techniques in CMOS

In analog CMOS design, offset is a fact of life! Even in modern processes, device mismatch typically results in offset voltages of several millivolts. But many analog circuits, e.g. precision amplifiers, sensor interfaces, and ADCs require much lower offset levels. Fortunately, by using dynamic offset-cancellation techniques such as auto-zeroing and chopping, microvolt levels of offset can be routinely achieved in standard CMOS. Compared to the alternatives, i.e. the use of huge devices or trimming, the use of dynamic offset-cancellation techniques has the added advantage of also reducing $1/f$ noise and drift, thus making it possible to design circuits that are thermal-noise limited. In this tutorial, an introduction to the basic theory behind auto-zeroing and chopping will be given, the pros and cons of both techniques highlighted, and recent advances in the state-of-the-art reviewed. Examples will be given of the use of auto-zeroing and chopping in CMOS circuits and systems with residual offsets as low as 50nV.

Instructor: Kofi A. A. Makinwa is an Associate Professor at Delft University of Technology, The Netherlands. He received the B.Sc. and M.Sc. degrees from Obafemi Awolowo University, Nigeria, in 1985 and 1988, respectively. In 1989, he received the M.E.E. degree from the Philips International Institute, The Netherlands, and then joined Philips Research Laboratories as a research scientist. In 2004, he received the Ph.D. degree from Delft University of Technology. He holds nine U.S. patents, has (co)-authored over 40 technical papers, and has given tutorials at the Eurosensors and the IEEE Sensors conferences. His main research interests are in the design of precision analog circuitry, $\Delta\Sigma$ modulators, and sensor interfaces. Dr. Makinwa has served on the technical program committees of the ISSCC, the International Solid-State Sensors and Actuators Conference (Transducers), and the IEEE Sensors conference. In 2005, he received the Veni and Simon Stevin Gezel awards from the Dutch Technology Foundation (STW), and was a co-recipient of the ISSCC 2005 Jack Kilby award.

T5: Error-Correcting Codes for Memories

Today's memories are increasingly susceptible to cosmic-ray-induced errors. In addition, lowering the supply voltage can increase circuit errors by reducing noise margin. Error-correcting code (ECC) can help solve both these problems by adding redundancy that allows recovery from errors. This tutorial starts from the basics of Shannon's theorem, and explores the need of ECC in nano-scale CMOS, soft errors in memory and basic coding such as Hamming code, cyclic code, and BCH code. It covers these topics in the context of modern memory, and their effect in advancing memory performance. The techniques are also applicable to high-speed logic.

Instructor: Takayuki Kawahara is a chief researcher at Central Research Laboratory, Hitachi Ltd. Since joining the laboratory in 1985, he has made fundamental contributions in many areas in the field of low-power memories, including subthreshold-current reduction by gate-source self-reverse biasing, an over-drive sense-amplifier scheme, and charge-recycling. Currently, his responsibility is to explore a new conceptual memory. He received B.S. and M.S. degrees in physics in 1983 and 1985, and a Ph.D. degree in electronics in 1993 from Kyushu University, Fukuoka, Japan.

T6: CMOS Front-End Circuit Design

In this turorial a general introduction covering system aspects of RF communication and relevant definitions, will be given. The tutorial covers CMOS RFIC design of low noise amplifiers LNAs and downconversion mixers. The circuit-design lecture first treats the modeling of CMOS devices including noise sources. Next, LNA and mixer design is presented from specifications to detailed topology discussions including all relevant aspects like impedance matching, noise figure, gain, bandwidth, linearity, and low-voltage design, without forgetting the crucial and critical RF ESD protection of LNAs. The circuits are illustrated through many measured test chip case studies aiming at RF standards from 1 to 20GHz.

Instructor: Marc Tiebout (S'90-M'93) received his M.S. degree in electrical and mechanical engineering in 1992 from the Katholieke Universiteit Leuven (Belgium) and the Ph.D. degree in electrical engineering from the Technical University of Berlin in 2004. In 1993, he joined Siemens, Corporate Research and Development, Microelectronics, in Munich, Germany, designing analog integrated circuits in CMOS and BiCMOS technologies. In 1997 he started the design of RF devices and building blocks in sub-µm CMOS technologies. From 1999 to 2005, he was with Infineon Technologies AG, Munich, Germany, where he worked on RF CMOS circuits and transceivers for cellular wireless communication products and conducted high-frequency RF CMOS research for 17 and 24GHz applications. Since March 2006, he is with Infineon Technologies Austria, Villach, acting as concept engineer for UWB front-end development. His main interest focusses on low-power high-frequency circuits and systems in CMOS. Marc Tiebout serves as a member of the technical program committee of ISSCC and ESSCIRC. He has authored and coauthored more than 30 IEEE publications.

T7: Vector Processing as an Enabler for Software-Defined Radio in Handsets

Wireless radio standards (for cellular, broadcast, connectivity, and positioning) are rapidly proliferating and continuously evolving. Accordingly, the trend in mobile handsets is toward multi-standard and multi-channel solutions (short term), and software defined radio (SDR) and cognitive radio (long term). The required baseband signal processing involves many giga operations per second, at a power budget of only a few hundred mW. In this tutorial we analyze the trade-off between the required flexibility (programmability) versus power consumption and die area for SDR. For a large class of baseband functions (including demodulation, channel estimation, equalization, interference cancellation, synchronization), programmable vector processing (SIMD) is presented as a key enabler for SDR. A number of vector processors are reviewed, ranging from products today to academic prototypes.

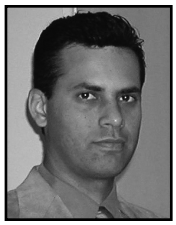
Instructor: Kees van Berkel is a Fellow at NXP Research in Eindhoven, the Netherlands. He received an M.S. degree (cum laude) in electrical engineering at the Delft University of Technology in 1980 and a PhD degree in computer science from the Eindhoven University of Technology (TU/e, 1992). Since 1996, he is a visiting Professor at the TU/e. During the 90s, he pioneered research on asynchronous VLSI circuits and contributed to their industrial application. Since the late 90s, his research focus moved to architectures for mobile wireless terminals. He initiated and co-architected the EVP, NXP's vector processor for modem applications. His current research interests include software-defined radio, signal processing algorithms, low-power vector DSPs, and interconnect-centric device architectures.

T8: Organic-Transistor Circuit Design

Organic transistors are expected to provide a way to build printable, flexible, and large-area electronic systems, which may open up new applications. This tutorial provides a comprehensive view of integrated circuit design approaches based on organic transistors. The tutorial covers organic IC examples like E-skin, sheet-type scanner, and Braille display.

- Technology aspect (process, structure, material, and encapsulation)
- Advantages and disadvantages
- Circuit design (modeling, and what are the differences from silicon)
- Coping with issues of low speed and reliability
- Applications and design examples
- Remaining issues and future directions

Instructor Takayasu Sakurai received the B.S., M.S. and Ph.D degrees in electrical engineering from University of Tokyo. In 1981, he joined Toshiba, where he designed numerous VLSI products including memories and processors. From 1988 to 1990, he was a visiting researcher at University of California, Berkeley. From 1996, he is a Professor at University of Tokyo, working on VLSI design and organic circuits. He was a conference chair and a TPC member of international conferences in the field of VLSI design including ISSCC, VLSI Circuit Symp., A-SSCC, CICC, ESSCIRC, and DAC. He is a recepient of 2005 IEEE ICICDT award, 2004 IEEE Takuo Sugano award, 2005 P&I patent of the year award, and other awards. He is an IEEE Fellow, a STARC Fellow, an elected AdCom member for the IEEE SSCS, and an IEEE CAS and SSCS distinguished lecturer.



T9: Radio Design for MIMO Systems with an Emphasis on IEEE 802.11n

Essential to the overall system design of a MIMO system, is the radio design. This course will provide a brief introduction to the legacy 802.11 a/b/g systems, followed by a discussion of the history of multiple antenna systems and the conventional analog-based techniques such as MRC. A general introduction to the 802.11n will then follow, which includes the channelization and modulation types, the definition and the description of the concepts behind the multiple spatial streams (MxN), and additional PHY and MAC techniques allowing for higher rates and/or longer reach. These features include the use of short guard-interval (GI), implicit and explicit beam-forming, space-time block codes (STBC), the use of Greenfield mode, and aggregation techniques. The requirements of 802.11n standard such as sensitivity and EVM and their relation to analog impairments such as phase noise, quadrature imbalances, linearity, and cross-talk will also be discussed. Some specific circuit examples will be presented and some unique circuit implementation challenges of MIMO radios will be discussed. Some measured performance numbers (range and throughput) will be also presented. The course will wrap up by discussing the future trends of MIMO radio implementation.

Instructor: Arya Behzad has worked in various senior circuit and system design capacities at various companies. Since 1998 he has been with Broadcom Corporation working on integrated tuners, gigabit Ethernet and wireless LAN systems and ICs. He is currently a Director of Engineering working on radios for current and future generation wireless products, and Product Line Manager for all Wireless LAN Radio products. He has over 70 patents issued and pending as well as many publications in the areas of precision analog circuits, cellular transceivers, integrated tuners, gigabit Ethernet, and wireless LANs. He has taught courses and presented technical seminars at various conferences and at several universities. Mr. Behzad is on his fifth year serving as a member of the ISSCC Wireless Technical Committee. He has served as a Guest Editor of JSSC and is currently an Associate Editor of the Journal. Mr. Behzad obtained his M.S. EE from UC Berkeley in 1994 after completing his thesis on the Infopad project.

T10: Fundamentals of Electronic Dispersion Compensation

Electronic dispersion compensation (EDC) has emerged as the technology enabling the migration of metro and long-haul optical fiber and backplane links to 10Gb/s to 40Gb/s rates. Both links suffer from various forms of dispersion or intersymbol interference (ISI), and noise. Fiber links also exhibit non-linearities due to fiber amplifiers and the photo-detector. The stringent power and throughput requirements have forced transmit and receiver ICs to be predominantly mixed-signal and the modulation to be binary. Meeting the challenges of designing next generation high data rate systems within a tight power budget requires the designer to understand the very basis of information transfer and go beyond the waveform shaping aspect exemplified by the 'eye-opening' techniques prevalent today. This tutorial will provide an overview of efficient transmit and receive techniques for both linear (back-plane) and non-linear (fiber) channels such as matched filtering, linear, decision-feedback, transmit techniques (pre-emphasis and partial response coding), maximum likelihood detector ('Viterbi equalizer') and their implications on mixed-signal design. The design of an OC-192 EDC chip-set will be presented as a case-study. Finally, the tutorial will conclude with a discussion on advanced topics and future directions.

Instructor: Naresh Shanbhag is currently a Professor in the Department of Electrical and Computer Engineering and the Coordinated Science Laboratory at the University of Illinois at Urbana-Champaign, Urbana, IL, USA. His research interests are in the area of low-power/high-performance integrated circuits and systems for DSP and communications. He is also a co-founder and Chief Technology Officer of Intersymbol Communications, Inc., (a wholly owned subsidiary of Kodeos Communications, Inc., since March 2006) Champaign, IL, USA, which was founded in 2000, and where he provides strategic directions in the development of EDC based mixed-signal receivers for next generation optical fiber links. He received his Ph.D. in EE from the University of Minnesota, located in Minneapolis, USA, in 1993. From 1993, Dr. Shanbhag worked at AT&T Bell Laboratories where he lead the development of its 51.84Mb/s VDSL chip-sets before joining the University of Illinois in 1995. Dr. Shanbhag became an IEEE Fellow in 2006, received the 2001 IEEE Transactions on VLSI Best Paper Award, the 1999 IEEE Leon K. Kirchmayer Best Paper Award, the 1999 Xerox Faculty Award, the Distinguished Lecturership from the IEEE Circuits and Systems Society in 1997, the National Science Foundation CAREER Award in 1996, and the 1994 Darlington Best Paper Award from the IEEE Circuits and Systems Society. From 1997 to 1999 and from 1999 to 2002, he served as an Associate Editor for the IEEE Transaction on Circuits and Systems: Part II and the IEEE Transactions on VLSI, respectively.

